CLAIM AMENDMENTS

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1. (Currently Amended) A digital signal processor comprising:

a programmable, multiply and accumulate ~~a~~ mathematical processor;

an input processor that processes input signals to the digital signal processor;

an output processor that processes output signals from the digital signal processor;

a master processor that controls said mathematical processor, said input processor and said output processor; and

a storage selectively accessible by each of said processors.

2. (Original) The digital signal processor of claim 1 further including a random access memory processor that stores intermediate calculation results.

3. (Original) The digital signal processor of claim 2 including a bus coupling each of said processors to said storage.

4. (Original) The digital signal processor of claim 1 wherein said input and output processors also implement mathematical operations.

5. (Original) The digital signal processor of claim 1 wherein each of said processors have their own instructions sets.

6. (Original) The digital signal processor of claim 1 wherein said processors communicate with one another through said storage.

7. (Original) The digital signal processor of claim 1 wherein each of said processors use very long instruction words.

8. (Original) The digital signal processor of claim 1 wherein said master processor provides the timing for the other processors.

9. (Original) The digital signal processor of claim 1 wherein said master processor waits for the input processor to complete a given operation.

10. (Original) The digital signal processor of claim 1 wherein each of said processors includes its own random access memory.

11. (Original) The digital signal processor of claim 1 wherein said storage includes a plurality of registers, said registers automatically transfer existing data from a first register to a second register when new data is being written into said first register.

12. (Original) The digital signal processor of claim 11 wherein said input processor causes the automatic transfer of data.

13. (Original) The digital signal processor of claim 11 wherein said mathematical processor causes said data to be transferred from one register to another.

14. (Original) The digital signal processor of claim 1 including a mathematical processor which is pipelined.

15. (Original) The digital signal process of claim 1 wherein said mathematical processor is a multi-cycled mathematical processor.

16. (Currently Amended) A method of digital signal processing comprising:

using a first processor to process input signals to said digital signal processor;

using a second processor to process output signals from said signal digital signal processor;

using a third processor for multiply and accumulate operations; ~~mathematical operations~~;

controlling said first, second and third processors using a fourth processor; and

enabling each of said processors to selectively access a storage.

17. (Original) The method of claim 16 including providing the timing from said fourth processor for each of the other processors.

18. (Original) The method of claim 16 including automatically transferring data from a first register in said storage to a second register in said storage when new data is being written into said first register.

19. (Original) The method of claim 18 including automatically transferring said data in response to action by said first processor.

20. (Original) The method of claim 18 including automatically transferring said data in response to action by said third processor.

21. (Original) The method of claim 18 including storing a bit which indicates which processor may control said automatic transfer of data from one register to another.

22. (Original) The method of claim 16 including accommodating for timing differences between said processors by operating one of said processor in a pipelined fashion.

23. (Original) The method of claim 16 including accommodating differences in processing cycle time of one of said processors by operating said processor in a multi-cycle mode.

24. (Original) The method of claim 23 including holding off said fourth processor when one of said processors is taking more than a cycle to complete an instruction.

25.-30. (Cancelled)